Performance Degradation due to Coupling between High-Speed Traces and On-Board Antennas

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***Abstract*—Self-interference between digital interfaces and on-board wireless modules and antennas is rapidly becoming a major problem for Printed Circuit Board engineers. In this paper, the severity of on-board self-interference is quantified. Two working conditions are considered. First, the situation is considered in which the antenna is in receive mode. As the incoming (signal) fields are most often rather low, only small (signal) voltages are induced at the antenna port. It is shown with a simple example that the level of the noise voltage induced at the antenna port due to the switching of digital interfaces can be significant compared to the signal voltage, thereby leading to a low Signal-to-Noise Ratio. Second, the situation is considered in which the antenna is in transmit mode. As the power radiated by the on-board antenna can be quite large (e.g. typically 2 Watt for GSM), the signal voltages at the antenna port can be quite large. With the same simple example, it is shown that this leads to a significant noise signal at the digital interfaces, thereby increasing the Bit Error Rate.**

I. Introduction

In the last years, wireless applications have seen an enormous increase. Not surprisingly, more and more devices have on-board multiple-input-multiple-output (MIMO) antennas. Designing and implementing such on-board wireless modules comprising multi-band antennas make Electro-Magnetic Interference (EMI) issues on Printed Circuit Boards (PCBs) even more complex problems than ever before [1]. Avoiding intra-system EMI or "self-jamming" has become one of the main problems that design engineers have to overcome.

In [2] and [3] it was shown that the overlap between antenna currents induced in PCB ground planes and return currents of critical digital traces is a good indicator for these intra-system interference issues. One of the first and most important rules to avoid interference on PCB level is to partition the PCB in an intelligent way, such that critical noise sources (e.g. high-speed digital circuits, memories,…) are placed far away from sensitive parts (e.g. analog receivers). The EMI reduction due to partitioning relies mainly on the physical phenomenon that above a few MHz return currents tend to stay very close to their signal current path, thereby minimizing the total current path's inductance. So, as long as this return current path is not disturbed, currents will be very "local" on the specified part of the PCB and will not interfere heavily with components at other places on the PCB. Unfortunately, on-board antennas can induce significant antenna currents in a large part of the PCB's ground planes, even in regions that are physically far away from the antenna. For successful partitioning of the PCB, the design engineer has to know the distribution of these antenna currents. During the placement stage of components on the PCB, the design engineer has to carefully select places where the digital interfaces will be placed, keeping in mind the antenna current profiles. Moreover, current path discontinuities have to be avoided. Simply stated, the design engineer has to make sure that there is as little as possible overlap between the antenna currents and the return paths of his digital interfaces. More overlap means a higher level of intra-system interference and visa versa.

In this paper, the work of [2] and [3] is extended by studying and quantifying the performance degradation that can be expected from self-interference between digital high-speed traces and on-board antennas. A simple example comprising a set of five microstrips and a folded multiband planar on-board antenna is used to show the performance degradation when the antenna is receiving and when it is transmitting.

This paper is organized as follows. Section 2 describes the design challenges that have to be overcome when integrating on-board antennas and discusses the typical signal levels that

can be expected at the antenna port in receive and transmit mode. Section 3 considers a practical example for the quantification of the self-interference. Finally, Section 4 draws concluding remarks.

II. Design Challenges Related to On-Board Antennas

During the design process of a PCB with on-board antennas, the PCB engineer is faced with two major challenges, which will be described below.

The first challenge is that these antennas have to be small, while still maintaining the required performance. Typical frequencies for which antennas have to be designed are 900 and 1800 MHz (GSM), 1.57 GHz (GPS), 2.4 GHz (Bluetooth, WLAN), and 5 GHz (WLAN). Due to their small physical size, these on-board antennas rely on the existence of a large ground plane on the PCB to aid in their performance [4]. As a result, the ground-plane shape (width, height, slots, holes,…) will have an influence on resonance frequencies and depths. This already makes it necessary to co-design the on-board antenna with the ground-plane. At the same time, antenna currents are induced in a very large part of the ground plane and can cause intra-system EMI problems in regions that are physically far away from the antenna location [2] and [3].

The second challenge is that modern PCBs contain a lot of high speed digital interfaces such as DDR2/3 memory bus or IO buses like USB3.0 (Universal Serial Bus) or HDMI (High-Definition Multimedia Interface) which can easily interfere with other parts on the PCB, certainly on-board antennas and their attached circuitry. When looking into more detail at the interference between digital interfaces and on-board antennas, one can conclude that the interference can actually happen in two ways, depending on whether the antenna is in receive or in transmit mode:

- If the antenna is in *receive mode*, it will have to be able to successfully receive and process very small signals. As the induced useful voltages at the antenna ports are typically very small, any noise that is induced at those ports leads to a significant decrease of the sensitivity of the receiver circuit. Hence, in receive mode, care has to be taken that the EMI coupling from the on-board digital circuits to the on-board antennas is kept small.
- If the antenna is in *transmit mode*, it will have to send out a significant amount of power (e.g. 2 Watt for GSM). This means that there are quite high voltages and currents at the antenna ports which can couple significantly to the digital interfaces thereby increasing bit error rates.

Below we will estimate the typical signal voltage levels at the antenna port for both the receive and transmit modes.

A. Typical signal levels in receive mode

Figure 1 shows the equivalent circuit representation of a receiving antenna. As was shown in [5], the open voltage source can be estimated based on the antenna's far-field pattern $\vec{E}_{\text{ff}}$ as:

$$V_{\text{open}} = -\frac{2j\lambda}{\eta}\frac{\vec{E}_{\text{ff}} \cdot \vec{E}_{\text{inc}}}{I_{\text{rad}}}, \tag{1}$$

where $\lambda = \frac{c}{f}$ is the wavelength and $\eta = 120\pi$ is the free-space intrinsic impedance. In (1), $\vec{E}_{\text{inc}}$ is the incoming field and I_{rad} is the current at the antenna port when the antenna is radiating. Hence, $\frac{\vec{E}_{\text{ff}}}{I_{\text{rad}}}$ represents the far-field pattern for the case where the antenna is excited with a 1A current source.

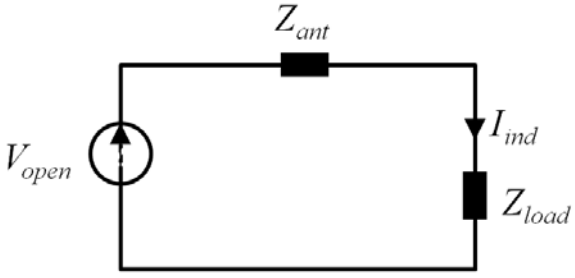


Fig. 1: Equivalent circuit of a receiving antenna

From Fig. 1 it follows that the induced voltage at the antenna ports is given by

$$V_{\text{rec}} = \frac{Z_{\text{load}}}{Z_{\text{ant}} + Z_{\text{load}}} V_{\text{open}}. \tag{2}$$

This allows us to make a rough estimate of the level that can be expected. As the on-board antennas are typically small compared to the wavelength, their far-field pattern will be very similar to that of a dipole. Therefore, a typical gain of 2dB (or expressed linearly 1.6) can be assumed:

$$G = 4\pi \frac{U(\theta,\phi)}{P_{\text{inj}}} \approx 1.6\,(2\text{dB}), \tag{3}$$

where $U(\theta,\phi)$ is radiation intensity (Watt/m^2).

Assuming that the antenna is matched to 50 Ohm, the power injected into the antenna port when excited with a current source of 1A can be estimated as follows:

$$P_{\text{inj}} = \frac{R_{\text{ant}}}{2} \approx 25\,\text{Watt}. \tag{4}$$

Further, the radiation intensity in a given direction is related to the far-field pattern in that direction as

$$U(\theta,\phi) = \frac{\left|\vec{E}_{\text{ff}}(\theta,\phi)\right|}{\eta}. \tag{5}$$

Consider as an example a GSM antenna working at 900 MHz and assume that Z_{load} is also 50 Ohm. Combining (1)-(5), one finds that the induced voltage (expressed in Volt) relates to the incident field (expressed in Volt/m) as

$$V_{\text{rec}} \approx 0.03\left|\vec{E}_{\text{inc}}\right|. \quad (6)$$

In [6], typical field values are given for the incident field for GSM communication. It is stated that one can expect electric fields with strength between 0.3V/m and 0.8V/m in indoor conditions and without a line-of-sight to the base station. In case of line-of-sight to the base station, one can excpect field strengths between 0.9V/m to 2.4V/m. Taking into account (6), this means that the signal voltage at the antenna port is in the order of 10 to 25 mV for indoor conditions and 25 mV to 75 mV if a line-of-sight with the base station is available.

B. Typical signal levels in transmit mode

In transmit mode, the power radiated by the antenna will be quite large. This radiated power can be related to voltage applied at the antenna port as:

$$V_{\text{rec}} = \sqrt{2R_{\text{ant}}P_{\text{rad}}}\,. \quad (7)$$

Taking again the example of GSM communication at 900 MHz with a maximum power of 2 Watt radiated by an antenna matched to 50 Ohm, the voltage at the antenna port can be as high as 14 Volt. This is excessive voltage an antenna has to provide and has reliability complications. Hence it is desired to keep power out as small as possible.

III. PRACTICAL EXAMPLE

In this section, the performance degradation due to self-interference between digital high-speed traces and on-board antennas is quantified by means of a combination of full-wave simulations and circuit simulations. All full-wave simulations below are done with the CUDA enabled Finite-Difference Time-Domain (FDTD) solver that is included in Agilent Technologies' 3D EM platform EMPro [7]. The circuit simulations are done with Agilent ADS [8].

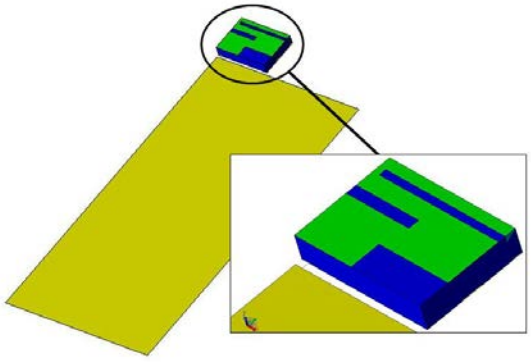


Fig. 2. On-board antenna under study

The on-board antenna used as an example in this paper is a folded, multiband planar monopole antenna whose design is inspired by the antenna described in [9]. This antenna is mounted at the top left corner of a single-layer PCB (Fig. 2). The design requirements were that the antenna should have good performance around 900 MHz and from 1.7 GHz up to 2.5 GHz. Moreover, it should fit within a volume of 20.0 mm by 8.0 mm by 4.0 mm. These are typical requirements for on-board antennas. The permittivity of the blue material supporting the antenna metallization is 2.2. Figure 3 depicts the insertion loss of this antenna between 0.5 and 3 GHz.

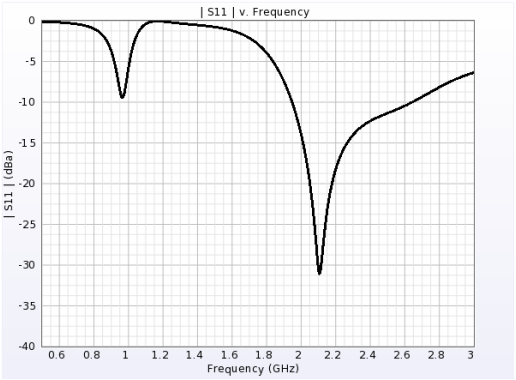


Fig. 3. Insertion loss of the on-board antenna

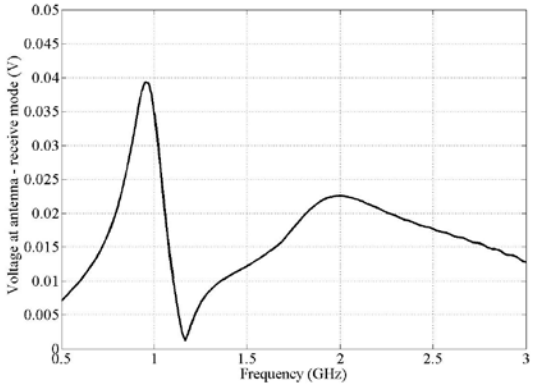


Fig. 4. Voltage induced at antenna port in receive mode for an incident plane-wave field of 1 V/m

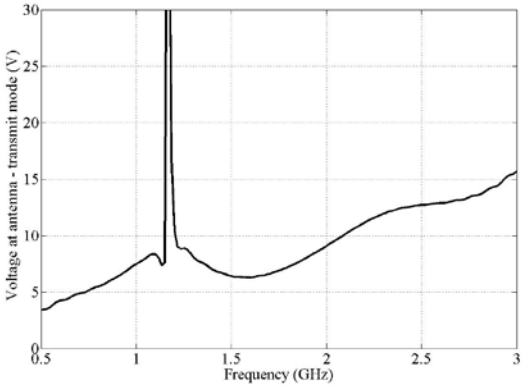


Fig. 5. Voltage induced at antenna port in transmit mode for a radiated power of 1 Watt

Based on the theory given in Section II, the maximum voltage induced at the antenna port for an incident (plane-wave) field of 1 V/m was calculated more accurately (Fig. 4). At 900 MHz, the induced voltage is around 35 mV for 1 V/m, which is close to the estimate of eq. (6).

Similarly, the voltage applied at the antenna port for a radiated power of 1 Watt was calculated (Fig. 5). Around 900 MHz, this is about 6 Volt for 1 Watt, which indeed gives about 10 Volt for 2 Watt, close to what was predicted based on eq. (7).

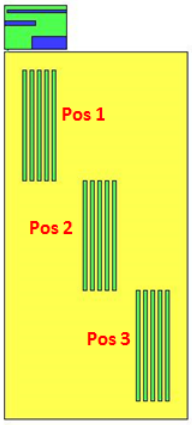


Fig. 6. Digital interfaces routed as microstrip lines at three different positions.

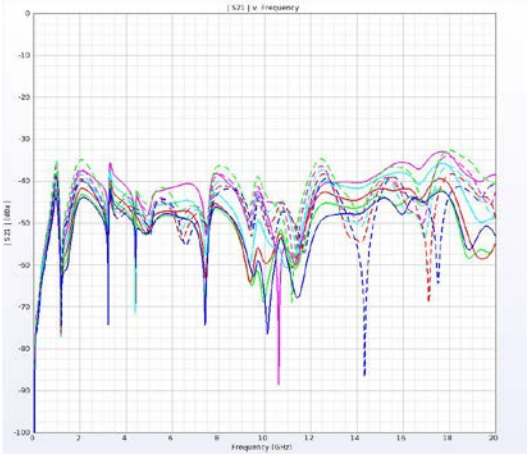
Figure 6 shows the first test-case that will be used to quantify the performance degradation due to the coupling between digital interfaces and the on-board antenna. The digital interfaces are modelled as five parallel 50 Ohm microstrip lines that are 5 cm long and spaced out by about 1 mm. They are positioned at three different locations: close to the antenna, half-way away from the antenna, and far away from the antenna.

Figure 7 shows the coupling (from DC to 20 GHz) between the traces and the antenna port for the three positions. Based on distance, one would expect that the coupling is the lowest for the case corresponding to interfaces placed far away from the antenna (position 3). However, this is not the case. For example, at 2 GHz, the coupling between the antenna and the interfaces in position 3 is almost as strong as that between the antenna and the interfaces in position 1. At 1.17 GHz, the coupling is low for all three cases. In [2],[3] it was proven that this can be explained by examining the antenna current distributions in the ground-plane for each position.

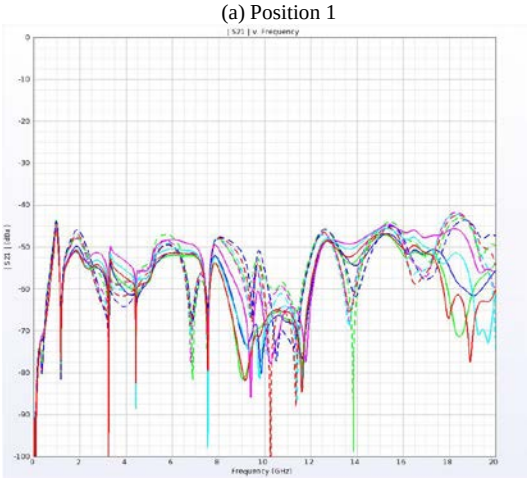
Next, these S-parameters are imported into ADS to quantify the typical noise levels in both receive and transmit modes.

A. Typical signal levels in receive mode

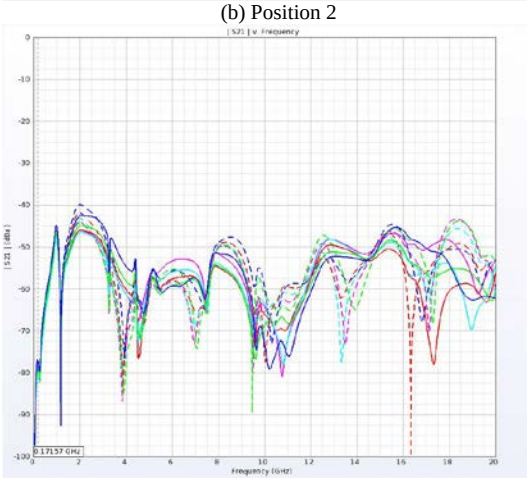
As explained above, in receive mode the coupling from the digital high-speed traces to the on-board antenna is important. To quantify this for the testcase in Fig. 6, all five microstrips were fed at the lower end with a pseudo-random bit sequence generator with a clock frequency of 1 GHz (0 Volt to 1.3 Volt, rise-time of 10 ps and fall-time of 15 ps). At the other end, every microstrip was loaded with 50 Ohm. The antenna port was also loaded with 50 Ohm.



(a) Position 1



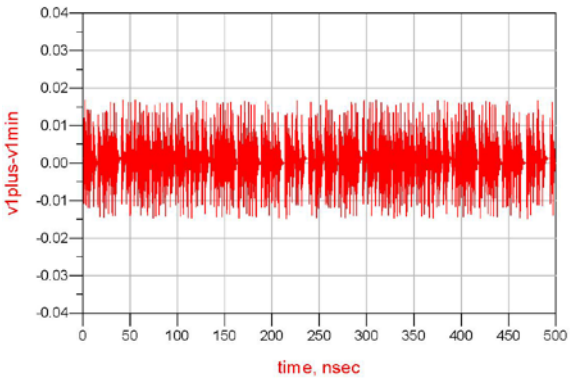
(b) Position 2



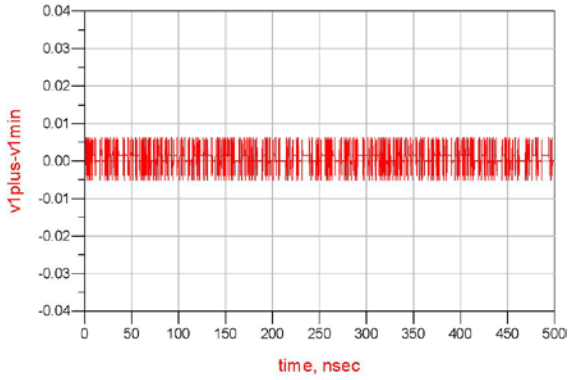
(c) Position 3

Fig. 7. Coupling from antenna to digital interface in Fig. 6.

Figure 8 shows the noise signals at the antenna port for the three positions. The maximum noise levels are around 5mV for position 2 and 15mV for positions 1 and 3. Compare this to the typical signal level of 35mV if 1V/m is falling in at 900 MHz. This situation becomes even much worse when the traces would be routed over a slot as shown in Fig. 9. Figure 10 shows that the noise level at the antenna port could be much larger than the typical signal voltage at the antenna port.



(a) Position 1



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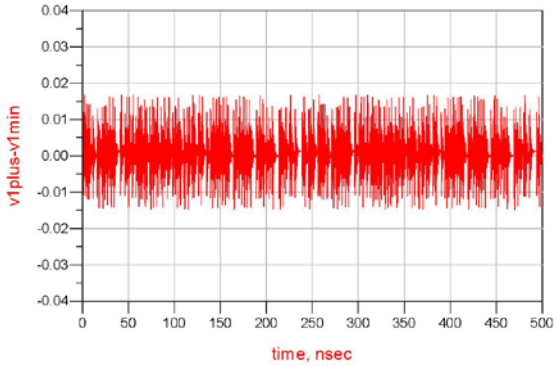


(c) Position 3

Fig. 8. Noise voltage at antenna port due to digital interfaces.

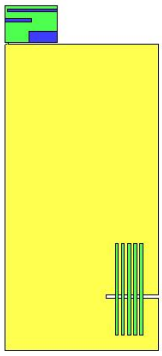


Fig. 9. Digital interfaces crossing a slot in the ground-plane

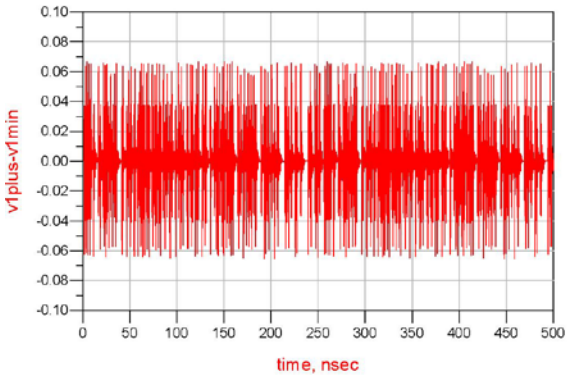


Fig. 10. Noise voltage at antenna port when microstrips in position 3 are routed over a slot.

B. Typical signal levels in receive mode

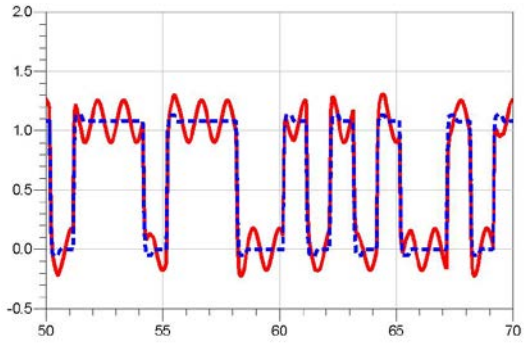
In receive mode, the coupling from the antenna to the digital traces is important. To quantify this, we apply a sinus source at 900 MHz with an amplitude of 10V (about 2 Watt radiated power) at the antenna port. A pseudo-random bit sequence generator was applied at one microstrip, while the voltage at the other end of the microstrip is monitored. Figure 11 shows this voltage for the three positions. The blue dotted curves represent the case where no signal is applied to the antenna port. The red solid curves show the case where a 10V signal is applied to the antenna in addition to the pseudo-random voltage source applied to the traces. Figure 12 shows the same quantity when the microstrips in position 3 are routed over a slot in the ground-plane. The effect of the slot in the ground plane is obvious in Figure 12. The antenna coupling is about 700mV when the slot is present. This is a large amount of untolerable noise which increases bit-error rates significantly in most digital buses.

IV. Conclusion

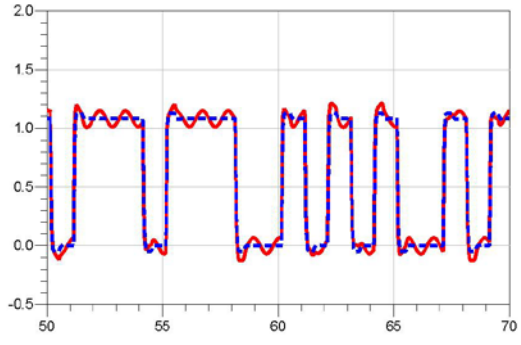
In this paper, the severity of on-board self-interference was quantified. Two working conditions were considered, namely receive and transmit mode for the on-board antenna. In receive mode the (signal) voltages induced at the antenna port are very low. It was shown with a theoretical consideration and with a simple practical example that the level of the noise voltage induced at the antenna port due to the switching of digital interfaces can be significant compared to the signal

voltage, thereby leading to a low Signal-to-Noise Ratio. In transmit mode, the power radiated by the on-board antenna can be quite large (e.g. typically 2 Watt for GSM) as well as the signal voltages at the antenna port. With a theoretical consideration and a simple practical example, it was shown that this leads to a significant noise level at the digital interfaces, thereby increasing the Bit Error Rate.

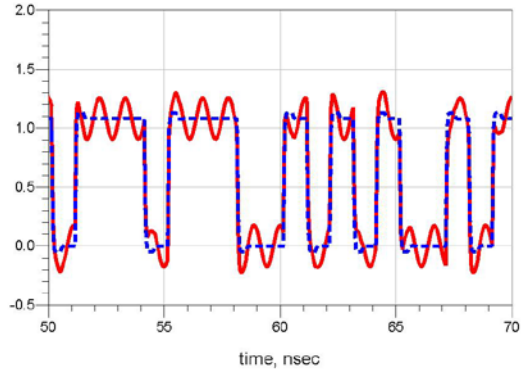
This paper has stressed once more that self-interference at PCB level is becoming a real issue which needs to be taken into account from the start of the design cycle. We also showed that both ways of interference (digital traces to antenna and antenna to digital traces) need to be considered.



(a) Position 1



(b) Position 2



(c) Position 3

Fig. 11. Voltage at load side of digital trace when no signal is applied to antenna port (dotted blue curve) and when a sinusoidal source of 10 Volt is applied in addition to the antenna port (solid red curve).

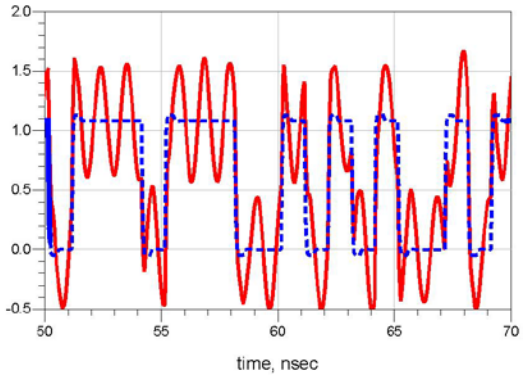


Fig. 12. Voltage at load side of digital trace routed over a slot when no signal is applied to antenna port (dotted blue curve) and when a sinusoidal source of 10 Volt is applied in addition to the antenna port (solid red curve).

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